Claims

1. An integrated semiconductor apparatus having
   - a large number of generators (G_A, G_B, G_X) for producing predetermined generator signals, with each of the generators (G_A, G_B, G_X) having a trimming unit with a trimming signal input (22_A, 22_B, 22_X) for receiving digital trimming data (TRM<i>), and the trimming unit being designed for trimming the generator signals that are produced, as a function of the trimming data (TRM<i>);
   - at least one fuse block device (10) having
     -- a large number of fuses (12) which are designed for nonvolatile storage of the trimming data (TRM<i>) for trimming the large number of generators (G_A, G_B, G_X),
     -- a parallel/serial converter (14) which is connected to the fuses (12) and to a timer (16) for signaling purposes and is designed to read the trimming data (TRM<i>) from the fuses (12) in parallel and to emit it in serial form via a fuse block trimming output (14_Q) to the fuse block device (14) in time (CLK) with the timer (16);

   in which
   - each of the generators (G_A, G_B, G_X) has a trimming signal output (28_A, 28_B, 28_X) and a large number of memory flipflops (24) which connect the trimming signal input (22_A, 22_B, 22_X) of the generator (G_A, G_B, G_X) to its trimming signal output (28_A, 28_B, 28_X), and
   - the memory flipflops (24) of the trimming units are connected to the fuse block trimming output (14_Q) in the form of a shift register chain for serial transmission of the trimming data (TRM<i>) from the

fuse block device (10) to the generators (G_A, G_B, G_X).

2. The integrated semiconductor apparatus as claimed in claim 1, in which the trimming signal input (22_A) is connected from one of the generators (G_A) to the fuse block trimming output (14_Q), and the trimming signal inputs (22_B, 22_X) of the other generators (G_B, G_X) are each connected in the form of a chain to one, and only one, of the trimming signal outputs (28_A, 28_B).

3. The integrated semiconductor apparatus as claimed in claim 1 or 2, in which the generators (G_A, G_B, G_X) are voltage generators and the generator signals are output voltages, and the trimming units are designed for trimming the output voltage as a function of the trimming data (TRM<i>).

4. The integrated semiconductor apparatus as claimed in claim 1 or 2, in which the generators (G_A, G_B, G_X) are delay generators and the generator signals are signals which are delayed in time with respect to a reference signal, and the trimming units are designed for trimming the time delay of the time-delayed signal as a function of the trimming data (TRM<i>).

5. The integrated semiconductor apparatus as claimed in one of the preceding claims, in which the fuse block device (10) has a fuse block clock output for emitting the clock (CLK) from the timer (16), and the fuse block clock output is connected to clock inputs (26_A, 26_B, 26_X) of the generators (G_A, G_B, G_X) for signaling purposes.

6. The integrated semiconductor apparatus as claimed in one of claims 1 to 4, in which the parallel/serial converter (14) is designed to emit the trimming data (TRM<i>) in a pulse-width modulated form.

7. The integrated semiconductor apparatus as claimed in one of the preceding claims, in which the fuses (12) are electrically or laser-programmable.

8. The integrated semiconductor apparatus as claimed in one of the preceding claims, in which the semiconductor apparatus is an integrated semiconductor memory.

9. The integrated semiconductor apparatus as claimed in one of the preceding claims, in which the semiconductor apparatus is an integrated logic circuit.